ISSN: 09742115
www.jchps.com Journal of Chemical and Pharmaceutical Sciences

# Switching mechanism for wireless PBX Using FPGA

**S. Beulah Hemalatha, M. Jasmin**
Department of ECE, BIHER
Bharath University
***Corresponding author: E-Mail: Beulah_s@gmail.com**

**ABSTRACT**

Switching is the fundamental operation in any Telecommunication system where two or more devices have to communicate with each other. This Project proposes the design of a low cost 4x4 switch network using FPGA, suitable for wireless PBX systems and Data transmission systems along with necessary equipment interfacing. The switch is simulated and implemented using the Xilinx Spartan 3/3E FPGA kit, and hence proves to be simple, scalable and flexible in operation and has low levels of Latency.

**KEY WORDS:** switch network, data wireless PBX systems.

## 1. INTRODUCTION

In a telecommunications network, a switch receives information from any of numerous info ports and transmits it to the predetermined port and takes the data towards the desired end point. In the routine telephonic system, one or many switches were used to create a dedicated but impermanent connection for data exchange between many clients. On an Ethernet LAN, with the help of the physical device addressor MAC address, a switch helps to determine to which output port the data should be forwarded and out of which input port the data has to be drawn. In the case of a WAN network like the Internet, using the protocol address a switch is used to find out which destination port has to be selected for the second phase of its travel to the desired destination.

FPGA is an incorporated circuit which contains over 10,000 similar logic cells.Every logic cell has its own personalities. Each cell can be interconnected with other cells using a switching logic. A user's design can be implemented by mentioning the simple logic function for each cell and then the switches in the interconnect matrix can be selectively closed. The fundamental component for any logic circuits is a fabric formed from an array of logic cells and interconnect. Design complexity are formed by interconnecting these fundamental components and creating the craved circuit. The switch designed using this FPGA makes programming easy, fast, flexible, and reduces latency.

**Literature survey:**

**Implementation of 4x4 crossbar switch for network processor – by anagha choudhari and prashant wanjari:** The network processor comprises of one main processor and multiple coprocessors that are connected to the main processor directly or indirectly through a shared bus. In this paper the implementation of a reconfigurability in the architecture of crossbar switches is proposed for the network processors. Primary focus of this paper is achieve increased performance, and high flexibility in a multiprocessor environment with network clusters. Final output shows VHDL simulation of Crossbar switches and its usage in the implementation of any broadcast function, present in message passing support middleware. Network Processors usually employ this reconfigurable crossbar Switch to connect the various circuits and to conduct the various tasks.

An NPU may include inbuilt coprocessors or otherwise can depend on external coprocessors. These coprocessors do not act as NPUs themselves. It comprises of three parts, the first unit is the Receive to Memory part (Rx2Mem) whose function is to count the number of bytes in the received frame and to determine its initial data byte. The next unit is the Control part, whose function is to forward frame data to the Process module and for storing both the received and the processed frames. Finally, the Process module is the third unit of the architecture, and is responsible for all the frame data processing by following all the instructions given in the design.

**Idea Evolved:** After studying the above papers on telecom & data switching, we intend to design a non-blocking switching network that can serve wireless communication as well as data communication. The chosen platform for the same is FPGA credited to its advantages mentioned in this report. The following content would explain the design requirements, hardware & software component specifications needed along with sample programs and results obtained during simulation using Xilinx ISE software and implementation of 2-bit data transmission using Spartan 3E FPGA kit.

**Hardware Required:**

**Proposed 4x4 switch design:** The design of the proposed switching network is such that it makes it suitable for telecom and Data transmission purposes. This system has 4 devices which can communicate with each other using six bi-directional Switches/Relays. The states of these six switches is controlled using the FPGA control depending on the inputs received from transmitting devices. The whole system is programmed using Xilinx ISE and Spartan 3 FPGA kit. The function of this switch is to route the incoming signal from the device to the destination device and enable data transmission between them.

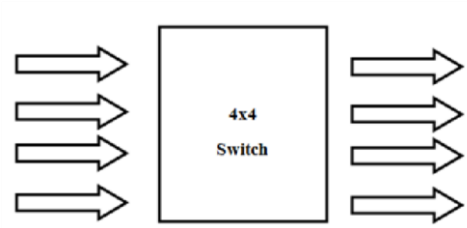


**Figure.1. 4x4 Switch**

**XCS250E FPGA:** FPGA is more advantageous over all general controllers .These FPGA's are economical and could be used for any applications starting from home appliances to industrial applications. In recent days these Microcontrollers are used in washing Machines, toys, Process Control equipment's, Printers etc.

FPGA XCS250E consists of an 32bit CPU, more no of timer/counters and I/O ports. XCS250E can access 2MB external program/data memory.

The VLSI board is based on XILINX XCS250E. It operates at 20 MHZ. The board can operate using the PC keyboard and 2 lines by 16-character LCD display and also with the PC (using the XILINX Software). **SM-VLSI Features:**

- FPGA operating at 20 MHZ
- 2MB RAM is available foe user XCF02S
- 26 pin FRC connector for user interface
- Timer and an external interrupt
- 101/108 PC type keyboard for entering user commands and address/data .
- Display purpose for using LCD
- Software monitor used for loading and program execution is more compatible to the users.
- Program download from kit to Pc using for JTAG with XILINX Software

**Hardware Description Of Spartan 3e:** SM-VLSI board XCS250E is useful to learn the basics of FPGA. The FPGA operates at 20 MHZ using a 20 MHZ crystal 1C 74LS373 is used for PWM Purpose.

Users can load their data or programs 2MB CMOS static RAM of type XCF02S.

Through the port pins, 101 PC type keyboard is interfaced to the Microcontroller. Microcontroller communicates with the keyboard using 2 wires- one for serial clock and one for serial data. LCD display can be directly linked to the bus. In this mode, port pins P82 and P83 act as receive and transmit pins. Baud clock is used for generating Timer 1. IC Max 232 convert TTL transmit and receive signals to RS 232 levels. Signals are then connected to a 9 pin connector.

FPGA has inbuilt counters or timers called timer 0 to 7.Baud clock is generated by Timer1. Timer 0 is available for the user.

Out of the five interrupts listed above external interrupt 1 TO 7 are available to the user.

SM-51L board is connected to the internal power supply

**Algorithm For The Switching And Data Transmission**

**Step 1:** Start the Program
**Step 2:** load the program onto the FPGA Kit.
**Step 3:** send the appropriate input to FPGA controller.
**Step 4:** Wait ,if the requested connection is Busy.
**Step 5:** After connection is established, Transmit the data.
**Step 6:** End the connection after the transmission is done.
**Step 7:** stop the program.

**Switch and Data Transmission**

**Switching and data transmission working:**

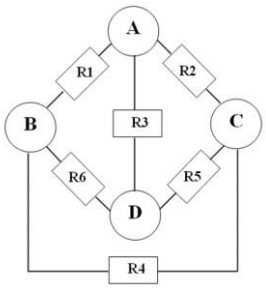


**Figure.2. Switch System Block**

This switching network consists of four devices connected to each other using six bi-directional switches or relays. These switches are closed by the FPGA controller depending upon the inputs it receives from any of the four devices. The resultant switch architecture is a non-blocking type of network where any transmitter can connect itself to any of the receivers, provided the receiver is not busy. Although if the receiver does not wish to make the connection it can do so and hence the transmitter will have to try later. After the requested connection is established, subsequently both the devices can exchange data between them. Such a system is optimum for applications in wired and wireless telecommunications.

The four devices can be designated as A, B, C and D. These devices send a 4-bit input or code which is taken by the FPGA controller as input to route that particular call/connection to the requested destination device.

**Coding Scheme:** For the purpose of our own understanding and programming, we assign two bit addresses to designate each device. Device A, B, C and D represented by 00, 01, 10 and 11 respectively. So for a connection from A to B, the FPGA takes a four bit input 0001. For connection from A to C the input is 0010. Similarly connection from A to D requires a input 0011 from the device A and connection from D to A will require a input 1100 from device D. Other connection are encoded in the similar fashion which is quite easy to understand and follow.

Switch R1 makes a connection between A and B, R2 between A and C, R3 between A and D, R4 between B and C. Switch R5 between C and D R6 between B and D. The reverse connections are also established using the same bi-directional switches. As indicated in the diagram, if a wishes to connect to B it sends a input of 0001 to the FPGA input port. Switch R1 gets switched ON if it is not busy and B can accept the connection and enable communication by sending common acknowledging code of 1111 to the controller.

Once connected, both the devices can exchange data as long as they want and at any point of time if A wishes to terminate the call/connection it sends common terminate code 0000 to the controller. During all this time devices C and D can communicate with each other similarly by sending the correct inputs to the FPGA controller, but none of them can connect to A or B as they will be busy. In short, any free device will be able to connect to any other free device.

**Truth Tables:**

| Input | Activated Switch | Connection State |
|---|---|---|
| 0000 | - | A Idle |
| 0001 | R1 | A -> B |
| 0010 | R2 | A -> C |
| 0011 | R3 | A -> D |
| 1111 | R1 or R2 or R3 | Data Transfer |

**Table.1. Truth Table for A**

| Input | Activated Switch | Connection State |
|---|---|---|
| 0000 | - | B Idle |
| 0100 | R1 | B -> A |
| 0110 | R4 | B -> C |
| 0111 | R6 | B -> D |
| 1111 | R1 or R4 or R6 | Data Transfer |

**Table.2. Truth Table for B**

| Input | Activated Switch | Connection State |
|---|---|---|
| 0000 | - | C Idle |
| 1000 | R2 | C -> A |
| 1001 | R4 | C -> B |
| 1011 | R5 | C -> D |
| 1111 | R2 or R4 or R5 | Data Transfer |

**Table.3. Truth Table for C**

| Input | Activated Switch | Connection State |
|---|---|---|
| 0000 | - | D Idle |
| 1100 | R3 | D -> A |
| 1101 | R6 | D -> B |
| 1110 | R5 | D -> C |
| 1111 | R3 or R6 or R5 | Data Transfer |

**Table.4. Truth Table for D**

**Simulation and test bench waveform:**

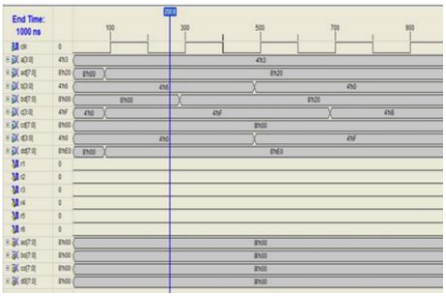

**Figure.3. Simulation Input Test Bench wave form**

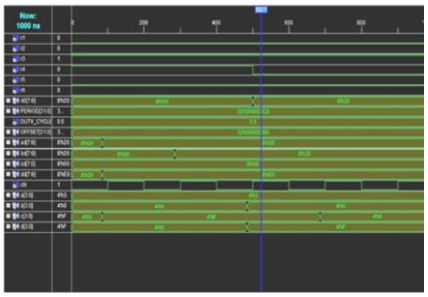

**Figure.4. Simulation Output**

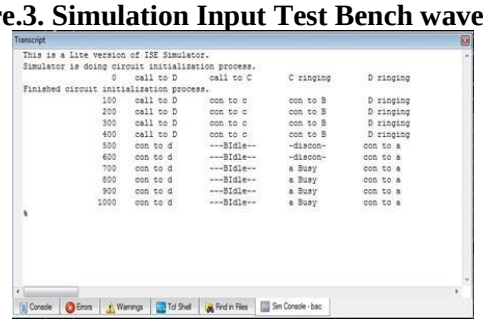

**Figure.5. Transcript output**

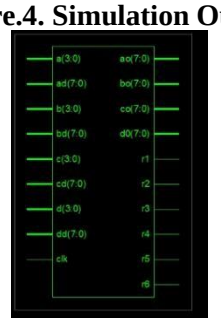

**Figure.6. RTL Schematic**

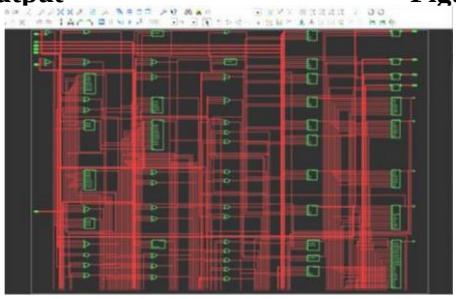

**Figure.7. Detailed RTL Schematic**

## 2. CONCLUSION

Thus a simple, unique and flexible 4x4 telecom/data switching system is designed and implemented using Spartan 3E kit. Such a system is low-cost, flexible and scalable for requirement in small communication networks such as wireless PABX and data communication systems.

**Future enhancement:** This project can be further enhanced by fusing of the above schematic into a chip. Further services like call waiting, conference call, and hardware implementation of busy tone can be added to it. Thus a complete low cost wireless pbx system can be built around our system with the help of analog FPGA fusing and by configuring wireless handsets to it.

## REFERENCES

Acampora A and Naghshineh M, An Architecture and Methodology for Mobile-Executed Handoff in Cellular ATM networks, IEEE Journal of Selected Area in Communications, 12(8), 1994 1365-1375.

Agrawal P, A Testbed for Mobile Networked Computing, In Proceedings of IEEE International Conference on Communications (ICC ‘95), 1995, 410-416.

Asthana A, Cravatts M and Krzyzanowski PAn Indoor Wireless System for Personalized Shopping Assistance, In Proceedings of IEEE Workshop on Mobile Computing Systems and Applications, 1994.

Barringer B, Infopad, A System Design for Portable Multimedia Access, Wireless, Calgary, Canada, 1994, 382-396.

Biswas S and Hopper A, A Connection Management Scheme for a Mobile Radio LAN, In Proceedings of the IEEE International Conference on Personal Wireless Communications, Bangalore, India, 1994.

Caceres R and Iftode L, The Effects of Mobility on Reliable Transport Protocols, In International Conference on Distributed Computing System, Cracow, Poland, 1994.

Chandler D.P, An ATM-CDMA Air Interface for Mobile Personal Communications, In Proceedings of PIMRC'94, 1994.

Gopalakrishnan K, Sundar Raj M, Saravanan T, Multilevel inverter topologies for high-power applications, Middle - East Journal of Scientific Research, 20(12), 2014, 1950-1956.

Jasmin M, Vigneshwaran T, Beulah Hemalatha S, Design of power aware on chip embedded memory based FSM encoding in FPGA, International Journal of Applied Engineering Research, 10(2), 2015, 4487-4496.

Kanniga E, Selvaramarathnam K, Sundararajan M, Kandigital bike operating system, Middle - East Journal of Scientific Research, 20(6), 2014, 685-688.

Kanniga E, Sundararajan M, Modelling and characterization of DCO using pass transistors, Lecture Notes in Electrical Engineering, 86(1), 2011, 451-457, 2011.

Karthik B, Arulselvi, Noise removal using mixtures of projected gaussian scale mixtures, Middle - East Journal of Scientific Research, 20(12), 2014, 2335-2340.

Karthik B, Arulselvi, Selvaraj A, Test data compression architecture for low power vlsi testing, Middle - East Journal of Scientific Research, 20(12), 2014, 2331-2334.

Karthik B, Kiran Kumar T.V.U, Authentication verification and remote digital signing based on embedded arm (LPC2378) platform, Middle - East Journal of Scientific Research, 20(12), 2014, 2341-2345.

Karthik B, Kiran Kumar T.V.U, EMI developed test methodologies for short duration noises, Indian Journal of Science and Technology, 6(5), 2013, 4615-4619.

Karthik B, Kiran Kumar T.V.U, Vijayaragavan P, Bharath Kumaran E, Design of a digital PLL using 0.35Î¼m CMOS technology, Middle - East Journal of Scientific Research, 18(12), 2013, 1803-1806.

Philomina S, Karthik B, Wi-Fi energy meter implementation using embedded linux in ARM 9, Middle - East Journal of Scientific Research, 20(12), 2014, 2434-2438.

Saravanan T, Sundar Raj M, Gopalakrishnan K, Comparative performance evaluation of some fuzzy and classical edge operators, Middle - East Journal of Scientific Research, 20(12), 2014, 2633-2633.

Saravanan T, Sundar Raj M, Gopalakrishnan K, SMES technology, SMES and facts system, applications, advantages and technical limitations, Middle - East Journal of Scientific Research, 20(11), 2014, 1353-1358.

Vijayaragavan S.P, Karthik B, Kiran Kumar T.V.U, A DFIG based wind generation system with unbalanced stator and grid condition, Middle - East Journal of Scientific Research, 20(8), 2014, 913-917.

Vijayaragavan S.P, Karthik B, Kiran Kumar T.V.U, Effective routing technique based on decision logic for open faults in fpgas interconnects, Middle - East Journal of Scientific Research, 20(7), 2014, 808-811.

Vijayaragavan, S.P, Karthik, B, Kiran Kumar, T.V.U, Privacy conscious screening framework for frequently moving objects, Middle - East Journal of Scientific Research, 20(8), 2014, 1000-1005.